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BAKER BOTTS L.L.P.
2001 ROSS AVENUE
SUITE 600
DALLAS, TX 75201-2980

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TREAT, WILLIAM M	
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ptomail1@bakerbotts.com
glenda.orrantia@bakerbotts.com

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/696,146
Filing Date: October 29, 2003
Appellant(s): GALLES ET AL.

Charles S. Fish
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/12/2011 appealing from the Office action mailed 5/12/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-20 are rejected and pending.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner disagrees with the applicant's summary of claimed subject matter contained in the brief. Applicant's summary of claimed subject matter is based on amendments to the figures, specification, and claims of the original disclosure. In the examiner's judgment the amendments represent new matter which is inconsistent with this applications original disclosure and the disclosure of application (09/418,520), now patent no. 6,651,157, which is the parent of this application.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

5,890,217	Kabemoto et al.	3-1999
6,374,331	Janakiraman et al.	4-2002

Gupta et al., "Reducing Memory Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes," In Proceedings of the International Conference on Parallel Processing, vol. 1, pp. 312-321, 1990.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants' have argued in the past that their claims are consistent with applicants' original disclosure and are not indefinite, citing Fig. 2 as their explanation. The following are the two points in applicants' specification where Fig. 2 is discussed.

On page 6, lines 9-10: "**FIG. 2 illustrates a block diagram of a processor within the multi-processor system**".

On page 8, line 24 through p. 9, line 31: "**FIG. 2 is a block diagram of a processor 12.** Processor 12 includes memory 16, a memory controller 30, memory directory 18, one or more network interfaces 32, and a CPU controller 34. Network interfaces 32 provide a communication capability between processor 12 and external switch 22. Memory controller 30 controls the read and write access from and to memory 16. CPU controller 34 controls flow between one or more processing units. The size of memory directory 18 may vary according to the size of its associated memory 16. For example, a processor 12 holding eight megabytes with sixty-four byte lines of cache in a four to one ratio may use 2(17) entries. Using a four gigabyte dynamic random access memory for memory 16, memory references may be represented by thirteen bit tags, two state bits, four pointer/vector bits and two error correction code (ECC) bits. With twenty-one bits per entry and 2(17) entries, memory directory 18 has a size of 2.6 Megabytes. As another example, a processor 12 holding thirty-two megabytes with one hundred twenty-eight byte lines of cache in a four to one ratio may use 2(18) entries. Using an eight gigabyte dynamic random access memory for memory 16, memory references may be represented by twelve bit tags, two state bits, four pointer/vector bits and two ECC bits. With twenty bits per entry and 2(18)

entries, memory directory 18 has a size of 5 Megabytes. With the presence of external directory 22, each memory directory 18 may be set up to track its local memory 16 cached memory references. External directory 22 may be set up to track remote cached memory references for the processors 12. Through the use of memory directories 18 and at each processor 12 and external directories 22 in a large multi-processor system 10 environment, cache coherency is provided to ensure that all processors 12 have an accurate view of the entire system memory. Requests for memory may even be passed from one external switch 14 to another to further extend the memory and access mechanism of multi-processor system 10."

In the examiner's judgment, applicants' Fig. 2 is an embodiment of a processor within the multiprocessor system as stated throughout their written description of Fig. 2. Arguments can be made that it is, instead, a CPU, but the plain fact is that applicants stated twice in their specification that Fig. 2 depicts a processor.

Applicants, on the other hand, have proposed changing their specification in the following manner:

Please replace the paragraph at page 8, line 24, beginning with "FIGURE 2 is a block diagram" as follows:

FIGURE 2 is a block diagram ~~of a~~ of central processing unit 20 of processor 12. Central processing unit 20 of processor ~~Processor~~ 12 includes ~~memory 16,~~ a memory controller 30 to interface with memory 16, memory directory 18, one or more network interfaces 32, and a CPU controller 34. Network interfaces 32 provide a communication capability between processor 12 and external switch 22. Memory controller 30 controls

the read and write access from and to memory 16. CPU controller 34 controls flow between one or more processing units. (5/23/2006)

Please replace the paragraph at page 6, line 2, beginning with "For a more complete understanding" as follows:

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like parts, in which:

FIGURE 1 illustrates a block diagram of a multi-processor system;

FIGURE 2 illustrates a block diagram of a central processing unit of a processor within the multi-processor system; and

FIGURE 3 illustrates a block diagram of an alternate embodiment of the multi-processor system. (10/6/2006)

Applicants have never submitted a proposed drawing change to change the “Bus Controller” legend to “CPU Controller” for element 34 of Fig. 2. In fact, in the 6.5 years since prosecution of the parent application (09/418,520) concluded with the issuing of Patent No. 6,651,157 on 11/18/2003 applicants have never sought to file a Certificate of Correction that would make the issued patent consistent in scope with the changes they propose for the child application. Applicants only sought to file amendments to the specification when the examiner made clear through 35 USC 112, 1st paragraph and 112, 2nd paragraph rejections of applicants’ claims, beginning on 9/23/2005, that their original disclosure did not support their invention as they had amended their claims to read.

Clearly, if Fig. 2 now becomes “a block diagram of a central processing unit of a processor” that is a change in scope from the parent application’s patent (6,651,157) which describes Fig. 2 as "a block diagram of a processor”. The other amendments applicants propose only magnify the difference in scope. The basic fact is that applicants’ original disclosure did not support their claims as they now read. The specification clearly did not support applicants’ claims. Applicants’ Fig. 2 is ambiguous, at best, because of reference numerals and legends that are inconsistent with the specification. Applicants only sought to amend the scope of their original disclosure when it was pointed out by the examiner their amended claim language, introduced to distinguish over Chase et al. (Patent No. 5,944,780) and Kabemoto et al. (Patent No. 5,890,217), was not supported by the scope of their original disclosure. The scope of applicants’ original disclosure does not support the claim language of independent claims 1 and 16 requiring, in substance, a CPU have a memory controller, as in claim 1, or a memory controller be integrated in the CPU, as in claim 16. For these reasons the examiner is unable to determine the true scope of the language of applicants’ claims 1-10 and 16-20.

Applicants argue in their appeal brief that their changes are only minor and clearly supported by Fig. 2 though the legends on the original drawing and the description in the original specification do not make clear this support.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scope of the term, “integrated”, was never defined by applicants' original disclosure in any clear way. One of ordinary skill might use it to mean that, for example, the memory controller is a part of the CPU and/or is on the same integrated circuit/chip as the CPU or is on the same board or is in the same cabinet, etc. One of ordinary skill might also use it to mean that the memory controller, which is a component of the processor system, works with the CPU which is another component of the processor system. Applicants seem to be leaving the scope of "integrated" purposely ambiguous while trying to amend the scope of applicants’ original disclosure to support a meaning for the term, “integrated”, which would require it to mean one element is a component of another element. There is nothing in their original specification that describes whether the CPU (20) and the memory controller (30) represent two boards, two chips, etc. or describes that the memory controller is part of the CPU. There appears to be some form of relationship between the directory (18) and the CPU (20) in Figs. 1 and 3, but what form that relationship takes is not made clear in applicants’ original disclosure. Applicants use the term, “integrated”, as though the meaning were well-defined by their original specification and has a uniform meaning in claims 1, 11, and 16 and as though the original specification supports such a uniform interpretation. Such usage renders the scope of the term, “integrated”, indefinite and therefore renders the scope of claims 1-20 indefinite.

In response to this rejection applicants argue the sentence, "Each of the plurality of processors 12 has a memory 16, a memory directory 18, and a central processing unit 20 all integrated into a single device” (page 7, lines 5-7), makes the meaning of the

term, integrated, as used in applicants claims and as argued in relation to the examiner's rejections of applicants' claims over the art, perfectly clear. In the examiner's judgment the sentence only says the various elements mentioned are integrated into a single system/device (i.e., they are all parts of a processor system and function together as components of a processor system). Applicants use the term, "integrated", as though the meaning were well-defined by their original disclosure and has a uniform meaning in claims 1, 11, and 16. Applicants arguments in response to the examiner's rejection of their claims over the art indicate applicant seeks to use phrases like "integrated memory" or "integrated memory controller" – claim 1, "integrated with" – claim 11, and "integrated in" – claim 16 to mean a high degree of physical proximity and physical interrelationship when applicants' original disclosure never makes clear whether the elements of applicants' drawings are in the same room, on the same circuit boards or board, on the same computer chips or chip, etc. The only relationship applicants' definition of integrated clearly supports for the elements of the processor system found in applicants' drawings and recited in the definition is that the elements work together as one processor system/device. Note that, originally, claims 1 and 11 never included the phrases cited, and claim 16 was not part of the original claim set. Such ambiguous usage of the term, "integrated", in a manner inconsistent with applicants' original disclosure, renders the scope of claims 1-20 indefinite.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-10 and 16-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The examiner is unable to find, in applicants' original written description, support for the claim language in claim 1 reciting "a central processing unit having an integrated memory controller operable to control access to the integrated memory or support for the claim language in claim 16 reciting "a memory controller integrated in the central processing unit and operable to control access to and from local memory". There is nothing supporting the claim to the CPU having such a memory controller though there is support for the processor having such a controller. For this reason the examiner views the quoted language as representing new matter.

The amendments to the specification filed on 5/23/2006 and 10/6/2006 are objected to under 35 U.S.C. 132(a) because they introduce new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: The amendments filed on those two dates as set forth, *supra*.

Applicants are required to cancel the new matter in the reply to this Office Action.

In relation to the rejections of applicants' claims 1-10 and 16-20 as new matter, the objection to the amendments to the specification as new matter, and the rejection of

applicants' claims 1-10 and 16-20 as being unclear because they are not consistent with the scope of the original disclosure, applicants have argued the numerical designation 18 for CPU pointing to an element in Fig. 2 instead of 12 for processor, the presence of a box labeled Directory within a box labeled CPU in other drawings, and the presence of the phrase, "Processor 12 includes memory 16" in the description when Fig. 2 does not show the memory in the box designated as 18 means Fig. 2 is a drawing of the CPU.

Were applicants inclined to see Fig. 2 as a drawing of an embodiment of a processor, the examiner is sure they would argue the 18 was a typo and should have been a 12. The fact Fig. 2 is described as a processor in the Brief Description of the Drawings and as a processor in the Detailed Description and never as a CPU is a clear indication of what Fig. 2 is meant to depict. Dropping the memory 16 from the description of an embodiment of a processor is as legitimate as dropping it from the description of a CPU, as applicants did in their amendments. Changing the detailed description of Fig. 2 to be a detailed description of a CPU when there are 7 mentions of a "processor 12" and none of a "CPU 18" makes no sense. Changing the scope of the written description so that it is no longer consistent with that of the parent application and the patent which resulted from the parent application makes no sense when a continuation-in-part (CIP) application under 37 CFR 1.53(b) is appropriate for such a change.

As pointed out by the examiner, there are credible arguments that Fig. 2 was meant to be an embodiment of a processor. As pointed out by applicants, one can also make arguments it was meant to be an embodiment of a CPU. It was applicants' duty

to file a written description which clearly described applicants' invention. That was not done. There was never a preliminary amendment filed correcting the parent which was filed on 10/15/1999. In the 6.5 years since prosecution of the parent application (09/418,520) concluded with the issuing of Patent No. 6,651,157 on 11/18/2003 applicants have never sought to file a Certificate of Correction that would make the issued patent consistent in scope with the changes they propose for the child application. Applicants only sought to file amendments to the specification when the examiner made clear through 35 USC 112, 1st paragraph and 112, 2nd paragraph rejections of applicants' claims, beginning on 9/9/2005, that their original disclosure did not support their invention as they had amended their claims to read. While the contradictory evidence and arguments make it impossible to determine what applicants really meant to describe in Fig. 2, it is clear that amending this application's specification to describe Fig. 2 as a CPU, when it was always described in multiple places in the specification of the parent and its resulting patent as a processor, means that such amendments constitute a significant change in scope and are new matter.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because of the inconsistencies between the specification and Fig. 2 noted in the 35 USC 112, 2nd rejection above. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be

labeled in the top margin as either “Replacement Sheet" or “New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Applicants argue the changes applicants propose are the appropriate ones despite the fact such changes would be inconsistent in scope with the patented parent application’s drawings and despite the examiner’s arguments.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-15 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kabemoto et al. (Patent No. 5,890,217).

The examiner would suggest applicants read col. 2, line 60 through col. 3, line 40; col. 16, line 5 through col. 20, line 40; and col. 28, line 55 through col. 29, line 10 and examine Figs. 2, 4, and 20, at a minimum, before responding.

To make clear how the examiner is interpreting applicants’ claim language the examiner is elaborating on his clearly anticipated rejection of claims 11-15.

Kabemoto taught the invention of claim 11 including: ***a method of accessing data in a multi-processor system*** (Figs. 2-4, and col. 2, line 67 through col. 3, line 40), ***comprising:***

storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system;

(Note that in **the embodiment of Kabemoto with only one CPU per processor module** ("FIG. 2 is a block diagram of a multiprocessor system to which a cache coherence apparatus of the present invention is applied. The system has, for example, five processor modules 10-1 to 10-5 as processor groups **each having at least one processor element**."– col. 16, lines 11-12), as depicted in Fig. 4, each processor group has the functionality of what applicants term a processor with CPU (34), memory management unit/controller (28), local memory (28), memory directory (30), and internal switch (32) coupled to an external switch (i.e., the switch (32) in another processor. Note that applicants are merely assigning the name, "processor", to a device with the same functionality Kabemoto teaches though Kabemoto might give the device another name. Given applicants use of broad terms in the art such as processor, memory, directory, and switch without any significant claim language to narrow the scope of such terms and their use of an unclear term such as integrated, the examiners interpretation of the Kabemoto reference is entirely consistent with his duty to afford applicants the broadest reasonable interpretation of their claim language when examining their claims.)

maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors;

(Col. 3, lines 14-40 -- It is inherent that the memory references in the memory directory (30) of Kabemoto would be maintained or his system could not function. Note that the examiner has interpreted the term, "integrated", to mean the CPU (34) works with the memory directory and both are components of a system/device which is consistent with one definition for integrated within the art and which inherently must occur if Kabemoto's system is to function. Applicants never supplied an alternative definition for the term in their original disclosure.)

maintaining at least one memory reference to information in the local memory of a different one of the plurality of processors in the memory directory integrated with the central processing unit of the particular one of the plurality of processors;

(Col. 18, line 51 through col. 20, line 18)

generating a request for data;

(Col 3, lines 14-40)

determining whether the data is associated with information stored in the local memory and has a memory reference in the memory directory;

(Col. 3, lines 14-40)

forwarding the request to an external switch in response to the data not having a memory reference in the memory directory, wherein the data not having a memory reference to the local memory in the memory directory is stored in a remote memory;

(Col. 3, lines 14-40 – As explained above, the examiner has interpreted the external switch (30) to be the switch (30) in another processor as opposed to the internal switch (30) of the requesting processor.)

identifying a memory reference for the data in response to the request;

(Col. 3, lines 14-40)

obtaining the data from the remote memory via the external switch in response to the identified memory reference.

(Col. 3, lines 14-40)

In response to this rejection of claim 11, applicant argues: "Independent Claim 11 recites ". . . ***storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system; maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors*** . . ."

By contrast, the Kabemoto, et al. patent shows processor and cache units separate from each other and a separate memory control module. Moreover, local memory 28 of the Kabemoto, et al. patent is shown to be associated with, but separate and apart from, it's four processor elements 14-1 to 14-4 in FIG. 3. Thus, the Kabemoto, et al. patent fails to disclose storing information in a local memory integrated within a particular one of a plurality of processors as required by the claimed invention. Further, a directory memory 30 is disclosed as being associated with, but separate and apart from, four processor elements 14-1 to 14-4 and their respective CPUs 34 in FIG. 3

of the Kabemoto, et al. patent. As a result, the processor elements and associated CPUs of the Kabemoto, et al. patent do not include the feature of a memory directory integrated with a central processing unit of a particular processor for maintaining a list of memory references to the information in the local memory within the particular processor as required by Independent Claim 11. Therefore, Applicant respectfully submits that Independent Claim ii is not anticipated by the Kabemoto, et al. patent.

First, applicants are arguing for an interpretation of the word, integrated, that requires a particular physical relationship of claim elements when, as the examiner has explained, previously, applicants original disclosure does not require such an interpretation nor support it. Second, applicants have failed to direct their arguments to **the embodiment of Kabemoto with only one CPU per processor module** ("FIG. 2 is a block diagram of a multiprocessor system to which a cache coherence apparatus of the present invention is applied. The system has, for example, five processor modules 10-1 to 10-5 as processor groups **each having at least one processor element** (i.e., each processor group can have only one processing element)."– col. 16, lines 11-12), as depicted in Fig. 4 and as explained by the examiner in his final rejection. Applicants directed their arguments to Fig. 3 which depicts a processor module with 4 processor elements in a processor module instead of the embodiment explained by the examiner. For these reasons applicants' arguments are irrelevant to the examiner's rejection of applicants' claim 11, and it stands rejected.

Though claims 11-15 stand or fall with rejected claim 11 based on applicants' failure to argue the other claims separately, the examiner is repeating his rejection of claims 12-15 as presented in his final action.

As to claim 12, Kabemoto taught "obtaining the memory reference to the data stored in the remote memory (Col. 19, lines 57-66; col. 20, lines 30-40; and Fig. 20).

As to claim 13, see the preceding rejection of claim 11.

As to claims 14 and 15, the memory reference which actually obtains the data which is returned to the local processor is generated in the home processor (Col. 19, lines 57-66; col. 20, lines 30-40; and Fig. 20).

For much of the more recent prosecution history the examiner has been arguing with applicants over the introduction into the disclosure of what the examiner views as new matter. The following rejection is to make clear that applicants' claims, even with the new matter, were not patentable over prior art at the time of applicant's invention.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janakiraman et al. (Patent No. 6,374,331).

Janakiraman taught the invention of claim 11 including: ***a method of accessing data in a multi-processor system*** (Fig. 8; col. 8, lines 7-9; and col. 8, lines 15-28), ***comprising:***

storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system;

(Fig. 8 and col. 8, lines 7-9)

maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors;

(Janakiraman shows a directory cache (2100, 3100, 4100, 5100) (also known in the art as a sparse directory) in Fig. 7 which reduces the latency for accessing the coherency directory by maintaining a small directory cache (2100, 3100, 4100, 5100) which indicates whether the memory line is exclusive, shared, etc. in the local memory (2010, 3010, 4010, 5010). This permits his system to supply memory data to the associated processor as soon as the directory cache (2100, 3100, 4100, 5100) indicates the data is valid without waiting for a response from the coherency controller/(communications switch) (6000, 7000, 8000). He also states that his system

maintains coherency between the directory cache (2100, 3100, 4100, 5100) and the coherency directory (6030, 7030, 8030) in the communications switch/(coherency controller) (6000, 7000, 8000 -- col. 7, lines 50-65). Janakiraman does not specifically teach that his directory cache (2100, 3100, 4100, 5100) is incorporated into his processor chip with the local memory and memory controller as depicted in Fig. 8 and as described in col. 8, lines 7-9. However, one of ordinary skill would recognize that the information provided by a directory cache (2100, 3100, 4100, 5100) is still useful in a system with the local memory and memory controller incorporated into the processor chip. The directory cache (2100, 3100, 4100, 5100) would reduce the latency by permitting the system to supply memory data to the associated processor as soon as the directory cache (2100, 3100, 4100, 5100) indicates the data is valid as opposed to waiting for the results of an access to the coherency directory (6030, 7030, 8030) in the communications switch/coherency controller (6000, 7000, 8000). Janakiraman makes clear that processor architecture and design trends were moving toward moving memory and memory controller onto the processor chip (col. 8, lines 7-15). Omitting directory caches (2100, 3100, 4100, 5100) from the system means the processor must wait for the slow access to the centralized coherency directory (6030, 7030, 8030) before knowing whether the local data is valid. Including the directory caches (2100, 3100, 4100, 5100) in a system with memory and memory controller on the processor chip but leaving the directory caches (2100, 3100, 4100, 5100) off-chip would largely negate the benefits from having faster on-chip access to memory because one would always have to make, at least, a slower access to the off-chip directory cache (2100,

3100, 4100, 5100) before knowing that the memory data was valid. One of the logical design options for one of ordinary skill would clearly be to bring the directory cache onto the processor chip with the other memory control elements thereby reducing latency associated with determining the validity of the data. Given that one makes such a design choice, the directory cache of Janakiraman would be integrated with the central processing unit (CPU) of Janakiraman's processor in every meaningful sense. The directory cache would certainly work with the processor's CPU. When CPU, memory controller, local memory, and directory, are all located on the same processor chip, one does not find little boxes etched on the chip with labels etched within the boxes saying CPU, etc. Various circuit elements may be in close proximity to one another on a chip to shorten the communications path between the elements, but the critical concept in determining whether two circuit elements are integrated is whether they work together. If drawing different boxes around circuits present on a computer chip or board, in a housing, etc., giving the boxes names, and terming them integrated constituted invention, any competent draftsman could render applicants' assignee's patents, IBM's patents, etc. useless.)

maintaining at least one memory reference to information in the local memory of a different one of the plurality of processors in the memory directory integrated with the central processing unit of the particular one of the plurality of processors;

(Col. 7, lines 57-61 – Janakiraman would be able to determine if the data were shared from his ccNUMA validity check. In other words, the information would also be

located in a different one of the plurality of processors. The examiner takes Official Notice of the fact that such directory information is a conventional design element in ccNUMA directory caches.)

generating a request for data;

(Fig. 6, and col. 7, lines 10-61)

determining whether the data is associated with information stored in the local memory and has a memory reference in the memory directory;

(Fig. 6, and col. 7, lines 10-61)

forwarding the request to an external switch in response to the data not having a memory reference in the memory directory, wherein the data not having a memory reference to the local memory in the memory directory is stored in a remote memory;

(Fig. 6, and col. 7, lines 10-61)

identifying a memory reference for the data in response to the request;

(Fig. 6, and col. 7, lines 10-61)

obtaining the data from the remote memory via the external switch in response to the identified memory reference.

(Fig. 6, and col. 7, lines 10-61).

Applicants argue in relation to the examiner's rejection of claim 11: "Claim 11 recites ". . . ***storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system; maintaining a list of memory references to the information in***

the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors . . ."

By contrast, the Janakiraman, et al. patent shows a memory controller 2520 separate from its processor 2540. Thus, the Janakiraman, et al. patent fails to disclose a memory controller integrated in the central processing unit and operable to control access to and from the local memory as required in Independent Claims 1 and 16. Further, the Janakiraman, et al. patent shows a coherency directory 6030 separate and apart from any of its processors 2540 and 3540. The Janakiraman, et al. patent also shows a directory cache being associated with two processors 2040 and 2050. Thus, the Janakiraman, et al. application fails to disclose a memory directory integrated with a central processing unit of a particular processor as required by Independent Claims 1, 11, and 16. The Examiner argues that it would be obvious to one of skill in the art from the Janakiraman, et al. patent to bring the directory cache on-chip. However, other than the Examiner's unsupported conclusory justification, there is no evidence of record from the prior art to support the leap the Examiner is making to justify the rejection of the claims on this point. Moreover, the Janakiraman, et al. patent teaches away from placing coherence control on the processor chip. The Janakiraman, et al. patent clearly states that it is not desirable to locate the coherence control on the processor chip collocated with the memory controller. See col. 8, lines 29-35, of the Janakiraman, et al. patent. Even assuming that one of skill in the art would make such a leap to bring a directory cache on chip, there is still no disclosure in the Janakiraman, et al. patent for having a memory directory in a central processing unit of a processor as required by the

claimed invention. Therefore, Applicant respectfully submits that Claims 1, 11, and 16 are patentably distinct from the Janakiraman, et al. patent.

As to applicants' argument that "the Janakiraman, et al. patent shows a memory controller 2520 separate from its processor 2540", the examiner would repeat his explanation that: "One of the logical design options for one of ordinary skill would clearly be to bring the directory cache onto the processor chip with the other memory control elements thereby reducing latency associated with determining the validity of the data. Given that one makes such a design choice, the directory cache of Janakiraman would be integrated with the central processing unit (CPU) of Janakiraman's processor in every meaningful sense. The directory cache would certainly work with the processor's CPU. When the CPU of the processor, memory controller, local memory, and directory, are all located on the same processor chip, one does not find little boxes etched on the chip with labels etched within the boxes saying CPU, etc. Various circuit elements may be in close proximity to one another on a chip to shorten the communications path between the elements, but the critical concept in determining whether two circuit elements are integrated is whether they work together. If drawing different boxes around circuits present on a computer chip or board, in a housing, etc., giving the boxes names, and terming them integrated constituted invention, any competent draftsman could render applicants' assignee's patents, IBM's patents, etc. useless.)".

As to applicants' argument that: "The Janakiraman, et al. patent also shows a directory cache being associated with two processors 2040 and 2050," the examiner would point out that there is a directory cache (2100, 3100, 4100, 5100) for each

memory controller (2020, 3020, 4020, 5020) in Fig. 7. When one has a memory controller (2510, 3510, 4510, 5510) for each processor chip as depicted in Fig. 8, it does not make sense for two processors to share an off-chip directory cache. As explained by the examiner, *supra*: "Omitting directory caches (2100, 3100, 4100, 5100) from the system means the processor must wait for the slow access to the centralized coherency directory (6030, 7030, 8030) before knowing whether the local data is valid. Including the directory caches (2100, 3100, 4100, 5100) in a system with memory and memory controller on the processor chip but leaving the directory caches (2100, 3100, 4100, 5100) off-chip would largely negate the benefits from having faster on-chip access to memory because one would always have to make, at least, a slower access to the off-chip directory cache (2100, 3100, 4100, 5100) before knowing that the memory data was valid."

As to applicants' arguments that: "The Examiner argues that it would be obvious to one of skill in the art from the Janakiraman, et al. patent to bring the directory cache on-chip. However, other than the Examiner's unsupported conclusory justification, there is no evidence of record from the prior art to support the leap the Examiner is making to justify the rejection of the claims on this point. Moreover, the Janakiraman, et al. patent teaches away from placing coherence control on the processor chip. The Janakiraman, et al. patent clearly states that it is not desirable to locate the coherence control on the processor chip collocated with the memory controller. See col. 8, lines 29-35, of the Janakiraman, et al. patent. Even assuming that one of skill in the art would make such a leap to bring a directory cache on chip, there is still no disclosure in the Janakiraman, et

al. patent for having a memory directory in a central processing unit of a processor as required by the claimed invention," the examiner would suggest rereading the examiner's rejection of claim 11 and his rejection of applicants' claims based on his unclear use of the term, integrated.

As to claim 12, Janakiraman taught: "the method of Claim 11, further comprising: obtaining the memory reference to the data stored in the remote memory" (Fig. 6, and col. 7, lines 10-61).

As to claim 13, see the rejection of claim 11.

As to claim 14, Janakiraman taught: "the method of Claim 13, wherein the identified memory reference is generated external to the particular one of the plurality of processors" (Fig. 6, and col. 7, lines 10-61).

As to claim 15, Janakiraman taught: "the method of Claim 13, further comprising: obtaining the data in response to the memory directory maintaining a memory reference to the data" (Fig. 6, and col. 7, lines 10-61).

As to claim 1, it differs from rejected claims 11-15 only in that the external switch of claim 11 is now integrated with an external directory that provides memory references for each processor linked to it to remote data. Janakiraman taught an external directory integrated with an external switch was prior art at the time of applicants invention (Fig. 6 and col. 7, lines 35-40 – "In the ccNUMA system 1000, since the coherence control and directory are maintained in the communication switch ..."). Such a design option could have been readily implemented by those of ordinary skill in the system of Fig. 8, too.

As to claims 4-9, 16-17 and 19, they fail to teach or define over rejected claims 11-15 and 1.

As to claim 10, Janakiraman taught: "the multi-processor system of Claim I, wherein the memory references in the external directory are represented in a same manner as memory references in a particular integrated memory directory" (Col. 7, lines 62-64 – "The directory cache and the coherence directory at the communications switch and coherency control can be maintained coherent." (i.e., in a same manner)).

Applicants only argue only their independent claims meaning the dependent claims rise or fall with the independent claims 1, 11, and 16. Since none of applicants independent claims are allowable, none of applicants' claims are allowable.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2-3, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janakiraman et al. (Patent No. 6,374,331) in view of Gupta (Reducing Memory and Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes).

Janakiraman taught the invention of independent claim 1 from which claims 2-3 and independent claim 16 from which claims 18 and 20 depend.

As to claim 2, Gupta taught those of ordinary skill, almost a decade before applicants filing, knew operating the integrated memory directory as a cache buffer reduced directory size thereby saving significant memory space (Section 1, Introduction) while suffering only minimal performance degradation (Section 6.3.1, Effect of Sparsity) and that the least-recently-used (LRU) algorithm was the best replacement policy for a directory cache (Section 6.3.2, Effect of Associativity and Replacement Policy, last paragraph, "LRU ... performs the best."). For these reasons Janakiraman would be motivated to implement the LRU algorithm in his directory cache.

As to claim 3, this is how the LRU algorithm of claim 2 inherently works.

As to claims 18 and 20, Gupta taught those of ordinary skill, almost a decade before applicants filing, understood the concepts related to sizing memories and directories (Section 4.2, Sparse Directories). Claims 18 and 20 are merely claims for size of a memory feature. Applicants have taught no new technology which results in a uniquely large size for their memory features. Absent such a teaching the size of the memory feature is merely a design choice readily implemented by one of ordinary skill.

Applicants argue claims 2-3, 18, and 20 are patentable over Janakiraman et al. (Patent No. 6,374,331) in view of Gupta (Reducing Memory and Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes) based on applicants' arguments that their independent distinguish over Janakiraman. As pointed out by the examiner, *supra*, applicants' independent claims do not distinguish over Janakiraman; therefore, claims claims 2-3, 18, and 20 are not patentable, either.

(10) Response to Argument

The examiner has responded to applicants' arguments as they relate to each rejection of applicants' claims at a logical point in each rejection of applicants' claims to provide context for the arguments and the response to the arguments. Se the previous section of the examiner's answer to review the arguments and response.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/William M. Treat/

Primary Examiner, Art Unit 2181

Conferees:

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2187